What is claimed is:

1. A power semiconductor device comprising a semiconductor chip in which a first main electrode, a second main electrode and a control electrode are formed, wherein:

a plurality of control electrode pads are provided on said semiconductor chip, said plurality of control electrode pads being disposed within the periphery of a gate area of said power semiconductor device, wherein said plurality of control electrode pads are connected to an electrode layer disposed outside said semiconductor chip via a conductive bonding member.

2. The power semiconductor device according to claim 1, wherein an active area of said power semiconductor device is formed between those of said plurality of control electrode pads of said power semiconductor device that are spaced apart from one another the most.

3. The power semiconductor device according to claim 1, wherein a center-to-center distance of said control electrode pads of said plurality of control electrode pads that are spaced apart from one another is not less than 1.5 mm.

4. The power semiconductor device according to claim 1, wherein said semiconductor chip comprises a first main surface and a second main surface, wherein said control electrode pads are disposed on said first main surface and said second main electrode is formed on said second main surface.

5. A power semiconductor device comprising a semiconductor chip in which a first semiconductor area forming a first main electrode, a second semiconductor area forming a second main electrode and a control electrode area forming a control electrode are formed, wherein:

a planar pattern is formed in said power semiconductor device, said

planar pattern comprising a repetition of unit patterns made up of said first semiconductor area, said second semiconductor area and said control electrode area, wherein said first semiconductor area in the repeating planar pattern is connected to a plurality of first main electrode pads, said control electrode area are connected to a plurality of control electrode pads, and said second semiconductor area is connected to a plurality of second main electrode pads, wherein said first main electrode pads are connected via a plurality of conductive bonding members to a metal electrode layer disposed outside said semiconductor chip, and wherein said second main electrode pads are connected via another plurality of conductive bonding members to another metal electrode layer.

6. The power semiconductor device according to claim 5, wherein said metal electrode layers and separated each other electrically, whereas they are formed on a same layer.

7. The power semiconductor device according to claim 5, wherein said control electrode area is connected via a first control-area conductive bonding member to a control-area metal layer disposed outside said semiconductor chip, and wherein the control-area metal layer is extended over its active area and connected to a second control-area conductive bonding member spaced from said first control-area conductive bonding member.

8. The power semiconductor device according to claim 5, wherein said semiconductor chip is a silicon semiconductor chip.

9. The power semiconductor device according to claim 5, wherein said semiconductor device is a power MOSFET in which said first main electrode is the source electrode, said second main electrode is the drain electrode, and said control electrode is the gate electrode of said power MOSFET.

10. A power semiconductor device comprising a power semiconductor device formed in a semiconductor chip, said power semiconductor device comprising a first control electrode pad for an external electrode, a second control electrode pad disposed away from said first control electrode pad, and a gate control circuit for said power semiconductor device, said gate control circuit being disposed between said first control electrode pad and the source of said power transistor, wherein said second control electrode pad is connected to the gate of said power transistor, and wherein said first control electrode pad is connected to said second control electrode pad via a conductive bonding member.

11. The power semiconductor device according to claim 10, further comprising an external control-electrode pad, wherein a control circuit for said power transistor is provided between said external control-electrode pad and said first control electrode pad, and wherein said first control electrode pad is connected to said second control electrode pad via a conductive bonding member.

12. A power semiconductor device comprising plurality of control electrode pads for the power semiconductor device formed within a semiconductor chip, wherein the control electrode pads are distributed within the periphery of the gate area.

13. The power semiconductor device according to claim 12, wherein the control electrode pads are connected via bumps or conductive bonding material to an electrode layer disposed outside the semiconductor chip.

14. A power semiconductor device, comprising
a semiconductor chip for which a plurality of power transistors with a plurality of pads for controlled electrodes of the semiconductor device,
a first electrode layer disposed outside said semiconductor chip, said first

electrode layer is contacted to said pads with conductive bonding materials.

15. The power semiconductor device according to claim 14, where the pad are formed apart from each other.

16. The power semiconductor device according to claim 14, said plurality of power transistors including a plurality of pads for source and/or drain electrodes of the semiconductor device,
second electrode layers different from said first electrode layer disposed outside said semiconductor chip, said second electrode layers is contacted to said pads for source and/or drain electrodes of said power semiconductor device with conductive bonding materials.